UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,154	10/10/2003	Saichirou Kaneko	50195-391	8202

7590 09/12/2006

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	**Application No.** 10/682,154	**Applicant(s)** KANEKO ET AL.	
	Examiner Thomas L. Dickey	**Art Unit** 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-31* is/are pending in the application.
  4a) Of the above claim(s) *4-7 and 10-19* is/are withdrawn from consideration.
5)☒ Claim(s) *20 and 30* is/are allowed.
6)☒ Claim(s) *1,8,9,21-24,28,29 and 31* is/are rejected.
7)☒ Claim(s) *25-27* is/are objected to.
8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☒ All b)☐ Some * c)☐ None of:
    1.☒ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 05/25/2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1,8,9,21-24,28, 29, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by TERASAWA (6,002,143).

With regard to claims 1,8,9,21,22,24,28, and 29, the specific embodiments of Terasawa's figures 8 and 13 disclose a tunnel-injection device, comprising a drain region 21-43 comprising a substrate 43 of a first (SiC) semiconductor, a reception layer 12 made of the first (SiC) semiconductor disposed on and metallurgically contacted with a top surface of the drain region 21-43; a barrier-forming layer 13 made of a second (polysilicon) semiconductor having a bandgap energy narrower than the first (SiC) semiconductor, being in metallurgical contact with the reception layer 12 so as to form a band-edge discontinuity barrier by a heterojunction interface between the first and second (polysilicon) semiconductors; a gate insulating film 14 disposed on the barrier-forming layer 13 contacting to the heterojunction interface; a gate electrode 15 disposed on the gate insulating film 14 configured to change a tunneling probability of the carriers, which are configured to be injected into the reception layer 12 by tunneling through the band-edge discontinuity barrier, by controlling a width of the band-edge, discontinuity barrier; a carrier-supplying region 16 (i.e. a source to match the claimed drain) made of the second (polysilicon) semiconductor, being contacted with the barrier-forming layer 13, configured to supply the carriers to the barrier-forming layer 13; and a source electrode 17 being contacted with the carrier-supplying region 16; and a drain electrode 48 (part #18 in figure 13) being metallurgically contacted with a bottom surface of the drain region 21-43; wherein the carrier-supplying region 16 and the barrier-forming layer 13 are laminated on the top surface of the reception layer 12, in a substantially same planar level; gate insulating film 14 contacts with the top surface of the reception layer 12 in a window part of the barrier-forming layer 13 being laminated on the top surface of the reception layer 12; wherein the first (SiC) semiconductor is made of SiC and the second (polysilicon) semiconductor is selected from the group consisting of single crystalline silicon, polysilicon and amorphous silicon, so that the second (polysilicon) semiconductor carrier-supplying region 16 and the second (polysilicon) semiconductor barrier-forming layer 13 are made of polysilicon films; and the barrier-forming layer 13 has a concaved sidewall on which the gate electrode 15 covers. Note figures 8 and 13, column 5 lines 37-67, column 10 lines 11-22, and column 11 lines 47-50 of Terasawa.

With regard to claim 23, the specific embodiments of Terasawa's figures 8 and 13 disclose a tunnel-injection device, comprising a source electrode 17 and a drain electrode 48 (part #18 in figure 13), main current flowing between the source 17 and drain 48 (part #18 in figure 13) electrodes, the tunnel-injection device comprising means 13 (Terasawa's barrier-forming layer 13 being an equivalent of the means disclosed in Applicant's specification) for prohibiting flow of carriers implementing the main current so as to establish cut-off state of the main current, by providing a band-edge discontinuity barrier; means 12 (Terasawa's reception layer 12 being an equivalent of the means disclosed in Applicant's specification) for providing a constant first band gap energy between the band-edge discontinuity barrier and the drain electrode 48 (part #18 in figure 13), and receiving the carriers injected by tunneling through the band-edge discontinuity barrier, being contacted with the drain electrode 48 (part #18 in figure 13); means (Terasawa's carrier-supplying region 16 being an equivalent of the means disclosed in Applicant's specification) for providing a constant first band gap energy between the band-edge discontinuity barrier and the drain electrode 48 (part #18 in figure 13), for providing a constant second band gap energy narrower than the first band gap energy between the source electrode 17 and the band-edge discontinuity barrier, and supplying the carriers so as to accumulate the carriers in front of the band-edge discontinuity barrier formed at the heterojunction interface between the first and second band gap energies, being contacted with the source electrode 17; and means (Terasawa's gate electrode 15 being an equivalent of the means disclosed in

Applicant's specification) for applying an electric field to the band-edge discontinuity barrier, the electric field narrows a width of the band-edge discontinuity barrier so that the tunneling probability of the carriers increases so as to establish conducting state of the main current. Note figures 8 and 13, column 5 lines 37-67, column 10 lines 11-22, and column 11 lines 47-50 of Terasawa.

With regard to claim 31, the specific embodiments of Terasawa's figures 8 and 13 disclose a tunnel-injection device, comprising a reception layer 12 made of a first (SiC) semiconductor; a barrier-forming layer 13 made of a second (polysilicon) semiconductor having a bandgap energy narrower than the first (SiC) semiconductor, being in metallurgical contact with the reception layer 12; a band-edge discontinuity barrier having a barrier height, on which carriers cannot (note paragraph 0063 of US Published Application No. 2004/0079989, wherein it is proven beyond any doubt that an SiC-polysilicon interface, such as the one found between Terasawa's first (SiC) and second (polysilicon) semiconductors, inevitably will form a band-edge discontinuity barrier having a barrier height, on which carriers cannot surmount. To quote 2004/0079989, "there is an energy barrier Δ_{Ec} ascribable to the difference of electron affinity of both silicon and SiC in the junction interface." 2004/0079989 antedates Applicants effective date but it is perfectly acceptable to use a reference that antedates an effective date for the purpose of showing an inherent property of something disclosed before said effective date. See *SmithKline Beecham Corp. v. Apotex Corp.*, 403 F.3d 1331, 1343-44, 74 USPQ2d 1398, 1406-07 (Fed. Cir. 2005); MPEP § 2112. Regretfully, when

Applicants filed their application in 2003 they could have had no way of knowing that the Federal Circuit was going to clarify the law of inherency in 2005) surmount, formed at a heterojunction interface between the first (SiC) and second (polysilicon) semiconductors; a gate insulating film 14 disposed on the barrier-forming layer 13 contacting to the heterojunction interface; a gate electrode 15 disposed on the gate insulating film 14 configured to change a tunneling probability of the carriers, which are configured to be injected into the reception layer 12 by tunneling through the discontinuity barrier, by controlling a width of the discontinuity barrier; and a carrier-supplying region 16 made of the second (polysilicon) semiconductor, being contacted with the barrier-forming layer 13, configured to supply the carriers to the barrier-forming layer 13. Note figures 8 and 13, column 5 lines 37-67, column 10 lines 11-22, and column 11 lines 47-50 of Terasawa.

Allowable Subject Matter

4. Claim 30 is allowed over the references of record for the reasons set forth in Applicants' paper filed 7/17/06. Claim 20 is allowed over these same references because it is a necessary method of making the product of claim 30.

5. Claims 25-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Primary Examiner
Art Unit 2826